Abstract of the Disclosure:

A test structure for determining the resistance of a conducting junction between an active region of a selection transistor and a storage capacitor in a matrix-type cell array where the active regions of the selection transistors are in rows in a first direction and the storage capacitors are in rows in a second direction running perpendicular to the first direction. The conducting junctions between the active regions of the selection transistors and the storage capacitors are formed at overlapping areas of the mutually perpendicular rows each in a single edge region of the overlapping area in the first direction. The active regions of the selection transistors and/or the storage capacitors are connected by tunnel structures or bridge structures in the second direction in the region adjoining the junction to be measured between the active region of the selection transistor and the storage capacitor. This achieves a low-impedance connection to the junction to be measured.

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